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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Application Number: 09/745,303

Filing Date: December 26, 2000

Appellant(s): SASAKI ET AL.

William L. Brooks

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/20/04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-4 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

1.	5,428,579	Robinson et al.	6/27/95
2.	6,332,196	Kawasaki et al.	12/18/01

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Robinson et al., U.S. Patent 5,428,579, in view of Kawasaki et al., U.S. Patent 6,332,196.

A) As to claims 1, 2, and 4, Robinson et al. discloses the invention substantially as claimed. There is a data reproduction device (the personal computer 101 shown in figure 1) that comprises a control circuit for reading out data recorded on a memory card (the "memory card" is shown as 110 in figure 1; the "control circuit" would be circuitry in personal computer 101 which would allow communication with the memory card when connected to the computer through connection 112) having a controller mounted thereon (Robinson et al. teaches at Col 5 Lines 10-12 that the memory card includes a controller. This controller can also be considered the "first control means to read out the data from

the memory card" which is claimed at line 10), and a data processing circuit for giving required processing to the read data and outputting the generated data (personal computer 101 contains a microprocessor/CPU that would be the "data processing circuit"). Robinson et al. also teaches that the controller of the memory card can operate the card under two current consumption modes, an active and a standby mode (see Col 2 Lines 6-12 and Line 50 to Col 3 Line 49). The memory card operates in the active mode when it is being read or written to and in the standby mode when no operation is occurring to the memory card. The standby mode operates with a non-zero current consumption for a second current value less than the first current value (see Col 9 Lines 3-54). This results in the same power savings as the present invention. However, Robinson et al. does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode.

Kawasaki et al. teaches a buffer that is utilized similarly to the claimed buffer. The buffer of Kawasaki et al. stores data from a storage device and when the buffer contains sufficient data the storage device is operated in a lower power mode. When the amount of data falls below a threshold the storage device is operated in an active mode and data is read into the buffer (see Abstract and Col 3 Lines 5-45). The buffer of Kawasaki et al. would also inherently include a "control means" to control reading from and writing to the buffer, thus meeting the "second control means to read out the data stored in the buffer" limitation at lines 11-12. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of

Kawasaki et al. in the system of Robinson et al. and provide a buffer between the memory card and the requestor of the data. The operation of the memory card would operate in a manner similar to that of the storage device taught by Kawasaki et al. When there is sufficient data in the buffer the memory card can be operated in a reduced power state, when the amount falls below a threshold the memory card would be operated in the powered up state (active mode) and data read into the buffer. This arrangement would provide power savings because the amount of time the memory card operated in a powered on state (active mode) would be decreased.

As for the limitation regarding "read out the data from the memory card at a first bit rate to store the generated data to the buffer ... read out the data stored in the buffer at a second bit rate less than the first bit" (Claim 1 Lines 10-12), these limitations would be inherently met by the teachings of Kawasaki et al. that are combined with the teachings of Robinson et al. There are only three scenarios possible with regard to the data transfer rates of the memory and that of the buffer:

1. memory date transfer rate < buffer data transfer rate
2. memory date transfer rate = buffer date transfer rate
3. memory date transfer rate > buffer date transfer rate

In order for the power savings Kawasaki et al. discloses to happen, the only scenario that can be true is the third one. With the first and second scenario the buffer would never fill up with data because it is being read out of the buffer at a greater or equal to date transfer rate than data is being read from the memory. This would mean that the memory would always be powered on in order to access more data. With the third scenario since the date transfer rate of the memory is greater then the date transfer rate of

the buffer, the buffer can be filled with data and then read from the buffer while the memory is powered down resulting in a power savings. Thus the combination of Robinson et al. and Kawasaki et al. would meet the claimed differences in bit rates of the memory and buffer as the claimed bit rates (buffer bit rate being less than the memory bit rate) is the only scenario possible that would allow for the power savings taught by Kawasaki et al.

B) As to claim 3, Robinson et al. teaches setting the memory card in the standby mode when there is no memory access within a predetermined period of time (see Col 16 Lines 16-24).

*(11) **Response to Argument***

Applicant argues that Kawasaki et al. teaches only one powered state, the other state consumes no power (see P 10 Lines 6-8). Applicant contends that this is in contrast to the present invention which teaches two power on states (see P 10 Line 9).

Robinson et al., *not Kawasaki et al.*, is relied upon for teaching a memory card that operates in two power on states. The memory card of Robinson et al. teaches both a powered on state and a standby mode, both modes being a "power on state" (i.e. non-zero current consumption). This is taught by Robinson et al. at Column 9 Lines 38-54 and is also agreed upon by Applicant's own Appeal Brief (see P 9). The fact that Kawasaki et al. does not teach two power on states is irrelevant since Kawasaki et al. was not relied upon for this feature of the claimed invention.

2. Applicant also argues that neither of the references teaches the relationship between the current consumption and the data transfer rates of the memory card and the buffer.

The Examiner addressed this issue in the Advisory Action mailed 3/10/04, paper number 15. The relationship between current consumption and data transfer rates would be met by the teachings of Kawasaki et al. that are combined with the teachings of Robinson et al. There are only three scenarios possible with regard to the data transfer rates of the memory and that of the buffer:

1. memory date transfer rate < buffer data transfer rate
2. memory date transfer rate = buffer date transfer rate
3. memory date transfer rate > buffer date transfer rate

In order for the power savings Kawasaki et al. discloses to happen, the only scenario that can be true is the third one. With the first and second scenario the buffer would never fill up with data because it is being read out of the buffer at a greater or equal to date transfer rate than data is being read from the memory. This would mean that the memory would always be powered on in order to access more data. With the third scenario since the date transfer rate of the memory is greater then the date transfer rate of the buffer, the buffer can be filled with data and then read from the buffer while the memory is powered down resulting in a power savings. Thus the combination of Robinson et al. and Kawasaki et al. suggests a relationship between the current consumption and the respective data transfer rates of the memory and the buffer.

3. Applicant argues at page 11 of the Brief that the Examiner asserted "that the data read out of the buffer in the stand-by mode is in intermittent bursts of 8 Mbps to result in an overall rate of 128Kbps" (Lines 8-9). The portion of the Office Action quoted by Applicant does not

make this assertion. The Examiner stated that the memory can provide data at 8 Mbps and that data being read out of the buffer is accessed at 128 Kbps. Obviously reading data from the buffer at 128 Kbps is not the same as reading the data at 8 Mbps. The external access of data at 128 Kbps compared to the speed at which the flash memory can provide data at 8 Mbps is comparatively an intermittent access. The "Summary of the Invention" provided in the Brief also states this, "the data is intermittently read out from the memory card 8 and stored in the buffer 2". In addition, there are no limitations in the claim of "128 Kbps" or "8 Mbps", so the specific speeds at which the flash memory or the buffer operate have no bearing upon the patentability of the claimed invention.

4. The Robinson et al. reference teaches operating a memory card in both an active and a standby mode in order to conserve power. The Kawasaki et al. references teaches utilizing a buffer memory between a storage device and a requestor so that the storage device can be placed into a reduced power state (see Col 3 Lines 11-13 and 19-21 of Kawasaki et al.) when data is being read out of the buffer. Utilizing the teachings of Kawasaki et al. in the system of Robinson et al. would mean providing a buffer for the memory card of Robinson et al. wherein when data is stored in the buffer the memory card could then be placed into a reduced power state. The reduced power state of the memory card of Robinson et al. is the standby mode, the same as the reduced power state of the present invention. Thus the combination of Robinson et al. in view of Kawasaki et al. teaches the claimed invention.

3. For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kevin L. Ellis

December 8, 2004

Conferees

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